RESPONSE

Claims 1-22 were pending in the Application. Claims 1, 3, 6, 8, 10, 13, 18, 19, and 22 are amended. Upon entry of the present Amendment, claims 1-22 are pending and presented for reconsideration.

Summary of Support For Claim Amendments

Support for the amendments to claims 1, 13, and 22 may be found in the Specification in, for example, paragraph [0076] on page 27. Support for the amendment to claim 3 may be found in the Specification in, for example, paragraph [0007] on page 3. Support for the amendment to claim 10 may be found in the Specification in, for example, paragraph [0079] and paragraph [0081].

Objections To The Specification

The Office Action objected to the word "Athalon" in paragraph [0034] and the phrase "redundant inputs" in paragraph [0043].

The Specification has been amended to correct the word "Athalon," which one skilled in the art would have recognized as an obvious typographical error for the word "Athlon." In particular, paragraph [0034] of the Specification has been amended to refer to "Athlon," as the Examiner suggested. Applicants respectfully submit that no new matter is introduced by the amendment of the Specification.

Applicants respectfully submit that the source and substance of the "redundant inputs" in paragraph [0043] of the Specification are clear from the context of paragraph [0043], the related paragraphs, and FIG. 3. Paragraph [0043] uses the phrase "redundant inputs" with respect to the comparator: "the I/O fault-tolerant logic 52 identifies errors when at least one of the inputs to the comparator 92 is different from the other, equivalent redundant inputs." Paragraph [0043] then states that the comparator is comparing I/O instructions: "the comparator 92 . . . performs a . . . comparison of the voted I/O instructions." Paragraph [0041] confirms that "the I/O fault-tolerant

logic 52 includes a comparator 92 that performs comparisons of the I/O instructions." Paragraph [0043] then makes clear that the I/O instructions come from redundant CPUs: "When the comparator 92 determines it received input data from each of the redundant CPUs 22 . . . ." Paragraph [0041] further confirms "the I/O fault-tolerant logic 512 compares the equivalent I/O instruction streams from each of the redundant CPUs 22 . . . ." Paragraph [0040] notes that "[i]n one embodiment, the I/O fault tolerant logic 52 communicates with the I/O bus interface 68 [whereas] in another embodiment, the I/O fault-tolerant logic 52 is implemented within the I/O bus interface 68." Applicants request that the objection to the phrase "redundant inputs" in paragraph [0043] be withdrawn since the source and substance of those redundant inputs is clear from the context.

Objections To The Claims

The Office Action objected to claims 3, 6, 8, 10, and 19 due to three distinct formalities. Claims 3, 6, 8, 10, and 19 have been amended to address the Examiner's objections.

The Office Action stated that it is unclear what "the CPU" refers to. Applicants amended claim 3 to clarify which CPU the claim refers to. As currently amended, claim 3 recites, in part, "a respective switching fabric in electrical communication with the respective CPU." Thus, each switching fabric referred to in claim 3 is in electrical communication with a corresponding CPU, as shown in FIG. 8 in which 22 and 22' are CPUs and 166 and 166' are switching fabric.

The Office Action identified an antecedent basis problem in claims 6, 8, and 19. Applicants amend claims 6, 8, and 19 consistently with the stated understanding of the Examiner. Applicants further amended claim 18 to address a similar issue.

Finally, in response to the Office Action's request for more clarity, Applicants amend claim 10 to clarify that a first delay module is in electrical communication with a first local I/O subsystem and a second delay module is in electrical communication with a second local I/O subsystem.

Therefore, the Applicants request reconsideration and withdrawal of the objections to claims 3, 6, 8, 10, and 19.

Rejections of Claims 1-22 Under 35 U.S.C. §112, First Paragraph

Claims 1-22 are objected to under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

Use of The Word "Instruction" In Claims

The Office Action states that the Applicants' use the word "instruction" in claims 1-22 to refer to the data that is compared, and then suggests that "there is strong evidence that the word is either being used contrary to the Applicant's intent or in a manner contrary to common understanding." (Page 3). The Office Action specifically suggests (a) that it is unclear if the word "instruction" refers to something that a CPU executes or generates, citing paragraphs [0004] and [0006] of the Specification; (b) that "[c]omparing instructions prior to execution" to ensure that they are substantially identical does not put CPUs in failover mode, citing paragraph [0029]; and (c) that "'instructions' are actually the output of the CPUs," citing paragraph [0044].

Applicants respectfully submit that one of ordinary skill in the art would understand the meaning of the word "instruction" when reading the word in its various contexts in combination with the teaching of the Specification taken as a whole. Applicants explain the various uses of the word "instruction" in Paragraph [0038] of the Specification:

> I/O instructions can be generated at each of the CPUs 22, or peripheral devices 42, and can be directed at any of the other CPUs 22 or peripheral devices 42. The I/O instructions include memory read or writes, configuration read or writes, mass storage device read or writes, or other special instructions.

Accordingly, a CPU may both execute and generate instructions. One of ordinary skill would understand from context which type of instruction is being referred to.

Applicants respectfully submit that CPU boards are configured in failover mode by executing substantially identical instructions as indicated in paragraph [0029] of the

Specification. "That is, at any instant in time, one CPU board 22, e.g., the second CPU board 22', remains ready to replace the first CPU board 22 upon a failure of the first CPU board 22." (Paragraph [0029]). Contrary to the suggestion of the Office Action, a CPU's proper processing of instructions is not identified by comparing instructions prior to their execution by CPU boards. Instead, the CPU failure test is accomplished by "compar[ing] the results of each operation performed by the separate CPU boards 22 to the results of the same operation performed on one of the other CPU boards 22', 22''." (Paragraph [0044]). If the I/O fault logic 52 determines there is a discrepancy, then a failure has occurred. (Paragraph [0043]). Thus, Applicants respectfully submit that the I/O fault-tolerant logic compares the results of CPU operations in failover mode to determine whether a CPU has failed.

Use of The Term "Substantially Equivalent" In Claims 6 and 18

The Office action suggests that the Applicants fail to disclose "how two instructions can be 'substantially' equivalent," as recited in claims 6 and 18. (Page 5).

Although Applicants believe that one of ordinary skill in the art at the time of filing of the application would understand "substantially equivalent" instructions, Applicants have amended claim 6 and claim 18 to eliminate the relevant word.

Applicants request reconsideration and withdrawal of the rejection of claims 1-22 under the first paragraph of 35 U.S.C. §112 because of the foregoing reasons.

Rejections Under 35 U.S.C. §102

Claims 1-10, 12-14, and 16-22 were rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,141,769 to Petivan et al..

Petivan

Generally, Petivan teaches a fault tolerant computer system that includes "a first system module with a first processor and a first processor bus and a first I/O bus; a second system

module with a second processor and a second processor bus and a second I/O bus; [and] a third system module with a third processor and a third processor bus and a third I/O bus." (Abstract). Petivan also teaches that each module includes a control device and comparison logic. (Abstract).

In Petivan's system, I/O controllers operate independently of each other and are not synchronized:

> [T]he I/O controllers of the TMR computer system operate independently of each other. They are not synchronized. That is, different operations may be initiated during the same time interval on the three I/O buses."

(Col. 4, lines 50-59).

Rejection of Independent Claim 1 Under §102 In View of Petivan

The Office Action suggests that Petivan anticipates all of the elements of original claim 1.

Claim 1, as currently amended, is a fault-tolerant server comprising:

(a) a communications link;
(b) a first computing element in electrical communication with the communications link, the first computing element providing a first instruction to the communications link;
(c) a second computing element in electrical communication with the communications link, the second computing element providing a second instruction to the communications link;
(d) a first local input-output (I/O) subsystem in electrical communication with the first computing element and the communications link; and
(e) a second local I/O subsystem in electrical communication with the second computing element and the communications link,

wherein at least one of the first local I/O subsystem and the second local I/O subsystem compares the first instruction and the second instruction and indicates a fault of at least one of the first computing element and the second computing element upon the detection of a miscompare of the first instruction and the second instruction, and

wherein the first local I/O subsystem is in electrical communication with the second local I/O subsystem via a sync bus to synchronize the first local I/O subsystem and the second local I/O subsystem.

Claim 1 has been amended to recite "a first local input-output (I/O) subsystem . . . ; and second local I/O subsystem . . . , wherein the first local I/O subsystem is in electrical

communication with the second local I/O subsystem via a sync bus to synchronize the first local I/O subsystem and the second local I/O subsystem." Support for the amendment to claim 1 may be found in the Specification, for example, in paragraph [0076] on page 27.

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest that "[a] first local I/O subsystem . . . in electrical communication with [a] second local I/O subsystem via a sync bus to synchronize the first local I/O subsystem and the second local I/O subsystem," as recited in amended claim 1. Thus, Petivan does not teach or suggest all of the elements of independent claim 1 as currently amended.

Rejection of Independent Claim 13 Under §102 In View of Petivan

The Office Action suggests that Petivan anticipates all of the elements of original claim 13.

Claim 13, as currently amended, is a method for a first computing element and a second computing element to execute in lockstep in a fault-tolerant server comprising:

> (a) establishing communication between the first computing element and a communications link;
> (b) establishing communication between the second computing element and the communications link;
> (c) transmitting, by the first computing element, a first instruction to the communications link;
> (d) transmitting, by the second computing element, a second instruction to the communications link; and
> (e) comparing, by at least one of a local input-output (I/O) subsystem of the first computing element and a local I/O subsystem of the second computing element, the first instruction and the second instruction and indicating a fault of at least one of the first computing element and the second computing element in response thereto,
>
> wherein the local I/O subsystem of the first computing element is in electrical communication with the local I/O subsystem of the second computing element via a sync bus to enable synchronization of the local I/O subsystems.

Claim 13 has been amended to recite "[a] local I/O subsystem of the first computing element is in electrical communication with [a] local I/O subsystem of the second computing element via a sync bus to enable synchronization of the local I/O subsystems." Support for the amendment to claim 13 may be found in the Specification, for example, in paragraph [0076] on page 27.

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest that "the local I/O subsystem of the first computing element is in electrical communication with the local I/O subsystem of the second computing element via a sync bus to enable synchronization of the local I/O subsystems," as recited in amended claim 13. Thus, Petivan does not teach or suggest all of the elements of independent claim 13 as currently amended.

Rejection of Independent Claim 22 Under §102 In View of Petivan

The Office Action suggests that original claim 22 is unpatentable in view of Petivan.

Claim 22, as currently amended, is an apparatus for enabling a first computing element and a second computing element to execute in lockstep in a fault-tolerant server comprising:

(a) means for establishing communication between the first computing element and a communications link;
(b) means for establishing communication between the second computing element and the communications link;
(c) means for transmitting, by the first computing element, a first instruction to the communications link;
(d) means for transmitting, by the second computing element, a second instruction to the communications link;
(e) means for comparing, by at least one of a local input-output (I/O) subsystem of the first computing element and a local I/O subsystem of the second computing element, the first instruction and the second instruction and indicating a fault of at least one of the first computing element and the second computing element in response thereto; and
(f) means for synchronizing the local I/O subsystem of the first computing element and the local I/O subsystem of the second computing element.

Claim 22 has been amended to recite "means for synchronizing the local I/O subsystem of the first computing element and the local I/O subsystem of the second computing element." Support for the amendment to claim 22 may be found in the Specification, for example, in paragraph [0076] on page 27.

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest "means for synchronizing the local I/O subsystem of the first computing element and the local I/O subsystem of the second computing element," as recited in claim 22 as currently amended.

Rejection of Dependent Claims Under §102 In View of Petivan

Applicants respectfully submit that claims 2-12, 14-21 are patentable because they depend on patentable independent claims (amended claims 1 and 13, respectively) as described above.

Therefore, in light of the foregoing reasons, Applicants respectfully request that the rejections under 35 U.S.C. §102 based on Petivan be reconsidered and withdrawn.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 11 and 15 under 35 U.S.C. §103(a) as being unpatentable over Petivan as applied to original claims 1 and 13. In particular, with respect to claim 11, the Examiner takes official notice of a 1U rack-mount form factor circuitry, such as a motherboard. In particular, with respect to claim 15, the Examiner takes official notice of error detection and correction in communications, examples of which are CRC, ECC, and parity.

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest that "[a] first local I/O subsystem . . . in electrical communication with [a] second local I/O subsystem via a sync bus to synchronize the first local I/O subsystem and the second local I/O subsystem," as recited in amended claim 1. Similarly, Petivan does not teach or suggest that "the local I/O subsystem of the first computing

element is in electrical communication with the local I/O subsystem of the second computing element via a sync bus to enable synchronization of the local I/O subsystems," as recited in amended claim 13. Thus, Applicants respectfully submit that claims 11 and 15 are patentable because they depend on patentable independent claims (amended claims 1 and 13, respectively).

Therefore, in light of the foregoing reasons, Applicants respectfully request that the rejections under 35 U.S.C. §103 be reconsidered and withdrawn.

SUMMARY

Claims 1-22 were pending in the Application. Applicants request that the Examiner reconsider the application and claims 1-22 in light of the foregoing Amendment and Response, and respectfully submit that the claims are in condition for allowance.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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